A mathematical model for an integrated self priming dielectric elastomer generator

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ABSTRACT

Dielectric Elastomer Generators (DEG) can capture energy from natural movement sources such as wind, the tides and human locomotion. The harvested energy can be used for low power devices such as wireless sensor nodes and wearable electronics. A challenge for low power DEG is overcoming the losses associated with charge management. A circuit which can do this exists: the Self Priming Circuit (SPC) which consists of diodes and capacitors. The SPC is connected in parallel to the DEG where it transfers charge onto/off the DEG based on changes in the DEG capacitance. Modelling and experimental validation of the SPC have been performed in the past, allowing design and implementation of effective SPCs which match a particular DEG. While the SPC is effective, it is still an external circuit which adds additional mass and cost to the DEG. By splitting the DEG into separate capacitors and using them to build an SPC, the Integrated SPC (I-SPC) can be realized. This reduces the components required to build a SPC/DEG and improves the performance. This paper presents a mathematical model with experimental data of a first order I-SPC. Additionally, comparisons between the SPC and I-SPC are drawn.

Keywords: Energy Harvesting, Dielectric Elastomer Generator, Self Priming, Low Power, Modelling

1. INTRODUCTION

Dielectric Elastomer Generators (DEG) are an excellent technology for harvesting energy from renewable sources. They are soft and flexible which allows them to be seamlessly integrated with natural motion sources.\textsuperscript{1} Such sources could be trees,\textsuperscript{2} water waves\textsuperscript{3-5} or human motion. A further benefit of DEG is their ability to generate at low excitation frequencies from stochastic sources; which is something other generator technologies typically struggle with (magnetic, piezoelectric).\textsuperscript{6-9} One of the challenges for DEG is the supply of high voltage charge which is required every generation cycle.\textsuperscript{10-12} An effective solution to this was presented by McKay et al. in the form of the Self Priming Circuit (SPC).\textsuperscript{13} This circuit consists of diodes and capacitors arranged in branches and then attached in parallel to the DEG, as shown by the first order SPC in Figure 1a. The SPC can be used to boost the DEG voltage from a low voltage up to the kilo volt range. Recently a mathematical model for the SPC has been presented which allows better understanding and optimization of the SPC, yielding higher amounts of generated energy.\textsuperscript{14,15} For the SPC to function at small amounts of strain, a higher order SPC is realized by adding parallel branches and modifying the capacitances of the SPC capacitors. Another modification to the original SPC presented by McKay et al.\textsuperscript{16,17} is the Integrated SPC (I-SPC) shown in Figure 1b. The I-SPC consists of four DEG connected with diodes in a similar fashion to a standard SPC, with the notable exception that the SPC's capacitors have been replaced with Dielectric Elastomers (DEs). Additionally, the I-SPC consists

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of two first order SPCs connected in parallel. In order for the I-SPC to achieve voltage boosting, the capacitance changes of the two separate SPCs must be out of phase by 180°.

![Schematic diagram of a 1st order SPC connected to a DEG](image1)

![Schematic diagram of a 1st order I-SPC](image2)

Figure 1

2. ELECTRICAL MODEL

In order to gain an understanding of how the I-SPC functions and to optimize its performance, a mathematical model is required. For this model all resistive losses (leakage, electrode resistance) are ignored and diodes are treated as ideal. It will be assumed that all the DE capacitors are of equal minimum capacitance $C_0$ and have an identical maximum swing $\beta_{\text{max}} = \frac{C_{\text{max}}}{C_0}$. Capacitances $C_{1A}$ and $C_{1B}$ are of equal amplitude and phase and are shown as $C_1$ in Figure 2a. Similarly, the capacitors of $C_2$ are shown to be of equal amplitude and in anti-phase with $C_1$. The capacitances can be represented in terms of minimum capacitance and instantaneous value of swing $\beta(t)$. In this derivation we will treat $C_1$ as the reference capacitance:

$$C_1(t) = \beta(t)C_0 \quad (1)$$

and thus $C_2$ is given by:

$$C_2(t) = C_0(1 - \beta(t)) + C_{\text{max}} \quad (2)$$

Where $\beta(t)$ is the time varying capacitance swing shown in Figure 2b. The swing has a minimum value of 1 which occurs when the DE is fully relaxed; and a maximum value of $\beta_{\text{max}}$ which occurs when the DE is fully stretched.

![Capacitance change for the DE membranes of a 1st order I-SPC](image3)

![The instantaneous swing $\beta$ used for the derivation.](image4)

Figure 2

We begin by charging the I-SPC to some initial voltage $V_0$. This occurs at time $t_0$ when $C_1$ is at its maximum capacitance, $C_{\text{max}}$ and $C_2$ is at its minimum capacitance $C_0$. The external voltage source causes diodes $D_2$ and $D_5$ to be forward biased which charges all capacitors to $\frac{V_0}{2}$ as shown in Figure 3a. By charging the I-SPC with an external source, we have introduced an initial state which during standard I-SPC operation would
not arise (Diodes $D_2$ and $D_5$ are never both conducting). During the transition from $t_0$ to $t_2$ the system will equilibrate itself to normal operating conditions. When the voltage source is removed, the voltage across the I-SPC immediately becomes $\frac{V_0}{2}$ as shown in Figure 3b as all capacitors could deliver current through diodes $D_1, D_3, D_4$ and $D_0$. The charge on each capacitor can be calculated at this time yielding:

$$Q_{C_1}(t_0) = \frac{V_0}{2} C_{\text{max}}$$  \hspace{1cm} (3)

$$Q_{C_2}(t_0) = \frac{V_0}{2} C_0$$  \hspace{1cm} (4)

![Circuit diagram](image)

(a) Circuit at time $t_0$. A DC source charges the DEGs in series through $D_2$ and $D_5$.

![Waveform diagram](image)

(b) Voltage and Capacitance waveforms of the I-SPC at time $t_0$.

Next the capacitance of $C_1$ will decrease while $C_2$ will increase. During this time diodes $D_1$ and $D_3$ are forward biased while all other diodes are reverse biased. This means that the system voltage is governed by the voltage of the $C_1$ capacitors. During the transition from $t_0$ to $t_1$ no current flows anywhere in the system and the voltage across the $C_1$ capacitors increases proportionally to its decrease in capacitance as shown in Figure 4b. At the same time, the voltage across the $C_2$ capacitors is decreasing in proportion to their increasing capacitance. At time $t_1$, the voltage on $C_{1A}$ and $C_{1B}$ will match the voltage of $C_{2A}$ and $C_{2B}$ added in series. This causes diodes $D_1, D_3$ and $D_5$ to conduct as $C_{1A}$ and $C_{1B}$ deliver charge to $C_{2A}$ and $C_{2B}$ in series as depicted in Figure 4a. To calculate the voltage $V_1$ at which this occurs, the value of swing $\beta_1$ is needed. This can be solved using the voltages on the capacitors:

$$V_1 = V_{C_1}(t_1) = 2V_{C_2}(t_1)$$  \hspace{1cm} (5)

Since no charge has flowed until this point, the charge on $C_1$ must be the initial charge as given by Equation 3 and using Equation 1 for the capacitance yields:

$$V_{C_1}(t_1) = \frac{Q_{C_1}(t_0)}{C_1(t_1)} = \frac{\frac{V_0}{2} C_{\text{max}}}{\beta_1 C_0}$$  \hspace{1cm} (6)

Similarly using Equations 4 and 2 for $C_2$ yields:

$$V_{C_2}(t_1) = \frac{Q_{C_2}(t_0)}{C_2(t_1)} = \frac{\frac{V_0}{2} C_0}{(C_0(1 - \beta_1) + C_{\text{max}})}$$  \hspace{1cm} (7)

And using Equations 6 and 7 in 5 and solving for $\beta_1$ yields:

$$\beta_1 = \frac{C_0 C_{\text{max}} + C_0^2}{2C_0^2 + C_0 C_{\text{max}}}$$  \hspace{1cm} (8)
This can now be used to solve $V_1$ yielding:

$$V_1 = V_{C1}(t_1) = \frac{V_0}{2} \left( \frac{2C_0 + C_{\text{max}}}{C_0 + C_{\text{max}}} \right)$$

\hspace{1cm} (9)

(a) Circuit at time $t_1$. Current begins to flow from $C_{1A}$ and $C_{1B}$ through diodes $D_1$ and $D_3$ charging $C_{2A}$ and $C_{2B}$ in series through $D_5$.

(b) Voltage and Capacitance waveforms of the I-SPC at time $t_1$.

During the transition from $t_1$ to $t_2$ current flows into $C_2$ from $C_1$ as described above until the capacitance of $C_1$ reaches its lowest value $C_0$. Conversely, $C_2$ has reached the maximum capacitance $C_{\text{max}}$ as depicted in Figure 5b. Current flow now ceases and the system voltage is controlled by $C_1$ through diodes $D_1$ and $D_3$ as shown in Figure 5a. Since no charge has been lost from the previous state, the voltage $V_2$ can be calculated from the total charge from the previous state, $Q_{\text{sys}}(t_1) = Q_{\text{sys}}(t_0)$ and the total capacitance at time $t_2$:

$$V_2 = \frac{Q_{\text{sys}}(t_1)}{C_{\text{sys}}(t_2)}$$

\hspace{1cm} (10)

From Equations 3 and 4, and consideration of the circuit at time $t_1$ we find:

$$Q_{\text{sys}}(t_1) = 2Q_{C1}(t_1) + Q_{C2}(t_1) = V_0C_{\text{max}} + \frac{V_0C_0}{2}$$

\hspace{1cm} (11)

The system capacitance is found by analyzing the circuit at $t_2$:

$$C_{\text{sys}}(t_2) = 2C_1(t_2) + \frac{1}{2}C_2(t_2) = 2C_0 + \frac{1}{2}C_{\text{max}}$$

\hspace{1cm} (12)

Using Equations 11 and 12 in 10 yields:

$$V_2 = \frac{V_0(C_0 + 2C_{\text{max}})}{4C_0 + C_{\text{max}}}$$

\hspace{1cm} (13)

(a) Circuit at time $t_2$. Current stops flowing and diodes end conduction.

(b) Voltage and Capacitance waveforms of the I-SPC at time $t_2$.

Figure 5

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As mentioned above, the I-SPC has been in an initial state which arose due to how it was charged at $t_0$. Normally the voltages of capacitors when they reach $C_{\text{max}}$ have a $2:1$ ratio rather than the equal ratio that arose in Figure 3a. Thus the expressions derived so far are valid only for the initial charging of an empty I-SPC.

Next we will derive the steady state operation of the I-SPC. During the transition from $t_2$ to $t_3$ no current flows anywhere in the circuit and the voltage of the system is again controlled by $C_1$. Thus the voltage slowly decreases as $C_1$ increases in capacitance as shown in Figure 6b. This continues until time $t_3$ when the voltage on the $C_2$ capacitors is higher than that of the $C_1$ capacitors. A switch over of system now occurs and the $C_2$ capacitors control the system voltage through $D_4$ and $D_6$ as shown in Figure 6a. To calculate the voltage at which this occurs, the value of swing $\beta_3$ is needed. This is solved by realizing that the voltages on all capacitors must be equal at time $t_3$:

$$V_3 = V_{C_1}(t_3) = V_{C_2}(t_3)$$

(14)

Since no charge has flowed during the transition from $t_2$ to $t_3$ the charge on $C_1$ is the charge from time $t_2$ yielding:

$$V_{C_1}(t_3) = \frac{Q_{C_1}(t_2)}{C_1(t_3)} = \frac{C_0V_2}{\beta_3C_0}$$

(15)

and similarly for $C_2$:

$$V_{C_2}(t_3) = \frac{Q_{C_2}(t_2)}{C_2(t_3)} = \frac{\frac{1}{2}V_2C_{\text{max}}}{C_0(1-\beta_3) + C_{\text{max}}}$$

(16)

Using Equations 15 and 16 in 14 yields:

$$\beta_3 = \frac{C_0 + C_{\text{max}}}{C_0 + \frac{1}{2}C_{\text{max}}}$$

(17)

This can now be used to solve $V_3$ yielding:

$$V_3 = V_{C_1}(t_3) = \frac{V_2}{\beta_3}$$

(18)

Next the circuit transitions from $t_3$ to $t_4$. During this time no current flows and the system voltage increases linearly as the capacitance of $C_2$ decreasing as shown in Figure 7b. At time $t_4$ the voltage on the $C_2$ capacitors will match twice the voltage of the $C_1$ capacitors. This causes diodes $D_2$, $D_4$ and $D_6$ to conduct as $C_{2A}$ and $C_{2B}$ charge $C_{1A}$ and $C_{1B}$ in series as shown in Figure 7a. To calculate the voltage $V_4$ at which this occurs, the value of swing $\beta_4$ is needed. This can be solved by relating the voltages on the capacitors:

$$V_4 = V_{C_2}(t_4) = 2V_{C_1}(t_4)$$

(19)
Since no charge has flowed since \( t_2 \) the charge on the \( C_1 \) capacitors must be this same charge. By using Equation 10 and 1 and consideration of the circuit at \( t_2 \):

\[
V_{C_1}(t_4) = \frac{Q_{C_1}(t_2)}{C_1(t_4)} = \frac{V_2 C_0}{\beta_4 C_0}
\]  

(20)

Similarly using Equations 10 and 2 for \( C_2 \) yields:

\[
V_{C_2}(t_4) = \frac{Q_{C_2}(t_2)}{C_2(t_4)} = \frac{\frac{1}{2} V_2 C_{\text{max}}}{C_0(1 - \beta_4) + C_{\text{max}}}
\]

(21)

Using Equations 20 and 21 in 19 and solving for \( \beta_4 \) yields:

\[
\beta_4 = \frac{C_0 + C_{\text{max}}}{C_0 + \frac{1}{4} C_{\text{max}}}
\]

(22)

This can now be used to solve for \( V_4 \) yielding:

\[
V_4 = V_{C_2}(t_4) = \frac{2V_2}{\beta_4}
\]

(23)

![Circuit diagram](image)

(a) Circuit at time \( t_4 \). Current begins to flow from \( C_{2A} \) and \( C_{2B} \) through diodes \( D_4 \) and \( D_6 \) charging \( C_{1A} \) and \( C_{1B} \) in series through \( D_2 \).

![Waveforms](image)

(b) Voltage and Capacitance waveforms of the I-SPC at time \( t_4 \).

Figure 7

During the transition from \( t_4 \) to \( t_5 \) current flows into \( C_1 \) from \( C_2 \) as described above until the capacitance of \( C_1 \) reaches its maximum value \( C_{\text{max}} \) as seen in Figure 8b. Conversely \( C_2 \) has reached its minimum capacitance \( C_0 \). Current now stops flowing and \( C_2 \) controls the system voltage through diodes \( D_4 \) and \( D_6 \) as shown in Figure 8a. Since no charge has been lost since the previous state, the voltage \( V_5 \) can be calculated from the total charge of the previous state \( Q_{\text{sys}}(t_4) \) and the total capacitance at time \( t_5 \):

\[
V_5 = \frac{Q_{\text{sys}}(t_4)}{C_{\text{sys}}(t_5)}
\]

(24)

From Equations 20 and 21 and consideration of the circuit at time \( t_4 \) we find:

\[
Q_{\text{sys}}(t_5) = Q_{C_1}(t_4) + 2Q_{C_2}(t_4) = V_2 C_0 + V_2 C_{\text{max}}
\]

(25)

The system capacitance is found by analyzing the circuit at \( t_5 \):

\[
C_{\text{sys}}(t_5) = \frac{1}{2} C_1(t_5) + 2C_2(t_5) = \frac{1}{2} C_{\text{max}} + 2C_0
\]

(26)
Using Equations 25 and 26 in 24 yields:

\[ V_5 = \frac{2V_2(C_0 + C_{\text{max}})}{4C_0 + C_{\text{max}}} \]  

(27)

This is the final voltage after a half cycle of steady state I-SPC operation. This expression can be simplified by substituting \( C_{\text{max}} = \beta_{\text{max}}C_0 \) which yields:

\[ V_5 = V_2 \frac{(2 + 2\beta_{\text{max}})}{(4 + \beta_{\text{max}})} \]  

(28)

Since time \( t_2 \) to \( t_5 \) is half a capacitance change cycle, a full cycle can be obtained by squaring the gain term \( G = \frac{(2 + 2\beta_{\text{max}})}{(4 + \beta_{\text{max}})} \) from Equation 28. Then if an initial voltage \( V_{\text{in}} \) and final voltage \( V_f \) are introduced, the following expression for a full capacitance change cycle is obtained:

\[ V_f = V_{\text{in}} \frac{(2 + 2\beta_{\text{max}})^2}{(4 + \beta_{\text{max}})^2} \]  

(29)

If an expression for \( k \) cycles is required, this can be further simplified and represented as:

\[ V_f(k) = V_{\text{in}} G^{2k} \]  

(30)

3. EXPERIMENTAL RESULTS

An I-SPC was constructed using the antagonistic membrane topology shown in Figure 9. This mechanism was driven by a motor with a reduction gearbox which converts the rotational motion into a linear stroke. The angular velocity of the motor was monitored by shaft encoder and closed loop control implemented with a half bridge to ensure a constant angular velocity.

Figure 9: Custom built linear reciprocating mechanism.
The mechanism produced a reciprocating motion of the linear guide which was then coupled to the DEG. Four DE membranes were painted on a pretrained (374% equibiaxially) VHB4905 membrane and a center plate was added to connect the membrane to the linear guide. When the motor of the mechanism was running, the guide stretched the DE membranes in a sinusoidal motion. These membranes were hand painted and as a result are not ideally aligned and geometrical, thus there are slight differences between capacitances. This slight mismatch of capacitance is visible from the geometry of the capacitors as shown in Figure 10. The mismatch was measured using a Hioki IM3523 LCR meter and was found to differ on average by 3%. While this mismatch is considerable, it was deemed acceptable for a preliminary test to evaluate the performance of the I-SPC.

![Figure 10](image1.png)

The previously derived model can now be compared to experimental and Spice simulation results. The experimental setup shown in Figure 9 and 10 had an average minimum capacitance \( C_0 \) of 1.4 nF and a maximum capacitance \( C_{\text{max}} \) of 3 nF. This yields a maximum swing \( \beta_{\text{max}} \) of 2.14. As is evident from the experimental capacitance readings shown in Figure 11a, there was some error between capacitances. They do however all have a very similar maximum swing and slight variations in minimum capacitance. The model and simulation however assume identical capacitances where \( C_1 \) is given by:

\[
C_1 = [0.8\sin(2\pi t) + 2.2] \text{nF} \tag{31}
\]

The DE membranes and GP02-40 diodes were connected up to form the I-SPC as shown in Figure 11b. An initial supply of charge was drawn from a 9 V battery which was then removed. Measurement of the system voltage was achieved with a custom built high voltage sensor circuit.

![Figure 11](image2.png)
An I-SPC with the capacitance change described in Equation 31 was implemented in Matlab and simulated in Spice. The experimental I-SPC was primed to a low voltage and subsequently boosted up to the 300 V range. At time = 0 in Figure 12a, the voltages of all traces are exactly 300 V and have been operating in steady-state operation for some time prior. As is evident, the Matlab and Spice simulation match very well with only a slight deviation as time continues. This arises due to the Spice simulation containing a real model for a diode while the mathematical model assumed an ideal diode with no forward voltage drop. The experimental results are similar to Matlab and Spice but have a lower voltage gain after every cycle as is evident from the voltage peaks in Figure 12a. There are a number of factors which cause this. The main factor was leakage resistance of the system, caused by monitoring equipment and DEG membrane leakage. The monitoring equipment used for this experiment has a constant resistance of \( \sim 5 \, \text{G\Omega} \) which would result in the capacitors that are currently controlling the system being discharged in \( \sim 70 \) seconds. This gives some idea as to how significant the losses on the system are. Thus it is not surprising when the experimental data is unable to boost as fast as theory predicts. Additionally, there was a slight difference in the peak voltage amplitudes when controlled by \( C_1 \) vs \( C_2 \). This effect is far more noticeable at higher voltages as show in Figure 12b. It is evident that due to these effects, model and simulation will quickly deviate from the experiment. While this indicates that the model requires the addition of loss elements, the performance of the loss-free I-SPC can still be compared to that of a loss-free SPC system.

![First Order I-SPC (LV Operation)](image1)

![First Order I-SPC (HV Operation)](image2)

**Figure 12**

### 4. COMPARISON WITH STANDARD SPC

With the standard SPC presented in other works, there is a minimum swing value required for the I-SPC to function.\(^{14,15}\) In this case, since the circuit is of first order (\( n = 1 \)), the swing required is \( > 2 \). And for higher order circuits the required swing is given by:

\[
\beta_{\text{max}} > \frac{n + 1}{n}
\]

In order to compare the ideal performances of the I-SPC and SPC, their voltage boosting and energy gain for a given volume of DEG will be evaluated. The system voltage for a standard first order SPC is given by:\(^{14}\)

\[
V_i = V_{i0} \frac{2(C_0 + C)(\beta_{\text{max}}C_0 + C)}{(2C + \beta_{\text{max}}C_0)(2C_0 + C)}
\]

Assuming the SPC has a single DEG with the same volume as used in the I-SPC experimental setup, it will have a minimum capacitance of \( C_0 = 4 \times 1.4 \, \text{nF} = 5.6 \, \text{nF} \). To compare voltage boosting it will be assumed the SPC is designed optimally for a particular swing value. Thus the SPC capacitance value \( C \) will be picked to optimize the voltage boosting performance. The value of \( C \) for an ideal SPC system has been presented in other works and is given by:\(^{14,15}\)

\[
C = C_0 \sqrt{\beta_{\text{max}}}
\]
Using this value of capacitance for the SPC and then inputting a varying value of $\beta_{\text{max}}$, the graph in Figure 13 can be produced. Since both of the circuits used here are first order, they produce no voltage gain below swings of 2. As is evident from the figure, the I-SPC has significantly higher boosting capabilities. This can be explained by the dual capacitance changes present in the I-SPC. Since the capacitance of the I-SPC is both increasing on one side and decreasing on the other, it reaches diode conduction periods sooner than the standard SPC. Additionally, the I-SPC has a swing doubling effect due to its anti-phase capacitances, and since the gain of these circuits is proportional to $\beta_{\text{max}}$, there is higher voltage boosting.

![Figure 13: Voltage boosting ability for first order SPC and I-SPC.](image)

Next we will consider the energy gain of both circuits. It will be assumed that the final voltage $V_f$ on each circuit is 600 V. The initial voltage $V_{in}$ is then calculated based on different values of swing using $V_{in} = \frac{V_f}{G}$. For the SPC, various values of capacitance $C$ are also considered. In theory the capacitors on each circuit are equally discharged so that in the following cycle they will again reach a $V_f$ of 600 V. The energy gain of each circuit is then given by:

$$E_{\text{gain}} = \frac{1}{2} C_{\text{total}} (V_f^2 - V_{in}^2)$$  \hspace{1cm} (35)

Where $C_{\text{total}}$ is found by considering each circuit at $V_f$ or $V_{in}$. For the I-SPC this is given by:

$$C_{\text{total}}(\text{I-SPC}) = 2C_0 + \frac{1}{2} C_0 \beta_{\text{max}}$$  \hspace{1cm} (36)

And for the SPC it is given by,$^{18}$

$$C_{\text{total}}(\text{SPC}) = C_0 + \frac{1}{2} C$$  \hspace{1cm} (37)

The initial voltages are then calculated from Equations 29 and 33. Figures 14a and 14b show the energy gains for I-SPC and SPC respectively. For the SPC, the capacitance values $C$ have been normalized with respect to the DEG capacitance. As is evident, the SPC has a higher energy gain if the capacitance $C$ is a few times larger than that of the DEG. While the energy gained will continue to increase as $\frac{C}{C_0}$ increases, the gained energy will flatten off at 0.5 mJ at very large values of $\frac{C}{C_0}$. This will result in low voltage boosting and a large impractical circuit. The I-SPC has better energy gain than the SPC for $\frac{C}{C_0}$ ratios of less than 5.5. Additionally, the I-SPC has a much higher voltage boosting capability that is not affected by attempts to produce more energy (increasing $\frac{C}{C_0}$). The combination of above factors make the I-SPC very compelling as an improvement to the standard SPC.
5. CONCLUSIONS

A model for a first order I-SPC has been derived and experimentally validated. Good agreement between simulation and model has been shown. Experimental results have shown basic agreement in system behavior but will require the addition of a loss term to the model before better agreement can be achieved. Comparison of the I-SPC to the SPC has been performed showing that for the same volume of DE material, the I-SPC has a superior voltage boosting ability. If the SPC is designed for harvesting large amounts of energy (C \gg C_0) it will out-perform the I-SPC slightly. This however comes at the cost of a large external capacitance and reduced voltage boosting. The SPC does have the advantage of “ideal” capacitors with low electrode resistance, making it easier to extract the generated energy. Future work will involve extension of the I-SPC model to higher orders and addition of loss to the model to improve agreement with experimental results.

6. ACKNOWLEDGMENTS

The authors wish to thank the Auckland Bioengineering Institute for their financial support during this research. This project has received funding from the European Union’s Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement No 706754.

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